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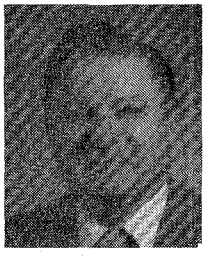
Dr. Vorhaus is a member of Phi Beta Kappa, Tau Beta Pi, and the American Physical Society.



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Dr. Pucel is a co-recipient of the 1976 Microwave Prize granted by the MTT Society. He also was the National Lecturer for the Microwave Theory and Technique Society for 1980–1981 on the subject of GaAs microwave monolithic circuits. In this role he lectured in the United States, Canada, Europe, the Middle East, and Asia, including the People's Republic of China.

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New Technology Towards GaAs LSI/VLSI for Computer Applications

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Abstract—**For future large-scale computer applications, new device technologies towards GaAs LSI/VLSI have been developed: self-aligned fully implanted planar GaAs MESFET technology and high electron mobility transistor (HEMT) technology by molecular beam epitaxy (MBE). The self-aligned GaAs MESFET logic with 1.5-μm gate length exhibits a minimum switching time of 50 ps and the lowest power-delay product of 14.5 fJ at room temperature. The enhancement/depletion (E/D) type direct coupled HEMT logic has achieved a switching time of 17.1 ps with 1.7-μm gate length at liquid nitrogen temperature and more recently a switching time of 12.8 ps with 1.1-μm gate HEMT logic, which exceeds the top speed of Josephson Junction logic and shows the highest speed of any device logic ever reported. Optimized system performances are also projected to system delay of 200 ps at 10-kilogate integration with GaAs MESFET VLSI, and 100 ps at 100-kilogate with HEMT VLSI. These values of system delay correspond to the computer performance of over 100 million instructions per second (MIPS).**

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I. INTRODUCTION

FUJITSU'S latest large-scale general purpose computer, using Si-based technology, has already achieved speeds as high as 30 Million Instructions Per Second (MIPS). In

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1990, the performance of 100 MIPS with the system delay per gate of 200 ps will be required [1], [2]. It may be difficult for Si-based technology to achieve these values. GaAs LSI/VLSI, however, seems the most promising device candidate to satisfy CPU and cache memory requirements for the mainframes of future computers.

For GaAs integrated circuits, three types of basic logic gates have already been developed: the Schottky diode FET logic (SDFL) gate [3], the buffered FET logic (BFL) gate [4], and the direct coupled logic (DCL) gate [5]. It has been demonstrated that LSI complexity can be achieved with the SDFL and the BFL gates with depletion- (D-) mode MESFET's. The largest scale of integration of SDFL circuits, an 8×8-bit binary multiplier with multiplication time of 5.3 ns, contains 1008 gates [6]. The largest of BFL circuits, 4-bit arithmetic logic unit (ALU) with high-speed digital processing time of 2 ns, in spite of 2-μm design rule technology, contains 99 gates [7]. To realize high-speed LSI/VLSI logic and memory for future computer mainframes, however, development of the DCL circuit with the enhancement- (E-) mode device would be desirable because of their circuit simplicity and low power dissipation.

This paper presents two advanced device technologies towards GaAs LSI/VLSI for computer applications: 1) self-aligned, fully implanted planar GaAs MESFET technology; and 2) high electron mobility transistor (HEMT) technology by molecular beam epitaxy (MBE). System delays of future computers, resulting from the device and wiring delays, are also projected and discussed.

II. Self-Aligned GaAs MESFET Technology

To realize the high-speed LSI/VLSI, the development of an E/D type DCL circuit with the fully implanted planar GaAs MESFET is very desirable. At present, the main problem is how to obtain reproducible characteristics of enhancement mode MESFET's. Both the instability of the Cr-doped semi-insulating GaAs substrate and the effect of surface depletion in the source–gate and gate–drain gaps resulting from surface states have to be solved. For the surface depletion problem, a very important breakthrough, i.e., self-alignment device technology, has been developed [8]. This technology was achieved, for the first time, by using the high-temperature stable TiW Schottky-gate metal system combined with ion implantation technology.

TiW films on GaAs stay unalloyed up to at least 860°C, and exhibit stable Schottky-diode characteristics even above 740°C. The self-aligned planar device utilizes this high-temperature stable metal for gate electrodes. Starting from wafers in which the MESFET N-channel implants have already been put in by selective implantation, four major stages in the self-aligned fabrication process are shown in Fig. 1. 1) The TiW Schottky gate is formed on n-type GaAs. 2) A high dosage Si^+ implantation is made with the gate acting as an implantation mask. 3) Annealing is carried out at 800°C for 10 min with SiO_2 encapsulation to activate dopants and to form the self-aligned n^+ regions. Gate electrical characteristics are not changed during the annealing process. 4) Fabrication is completed by ohmic metallization with AuGe/Au.

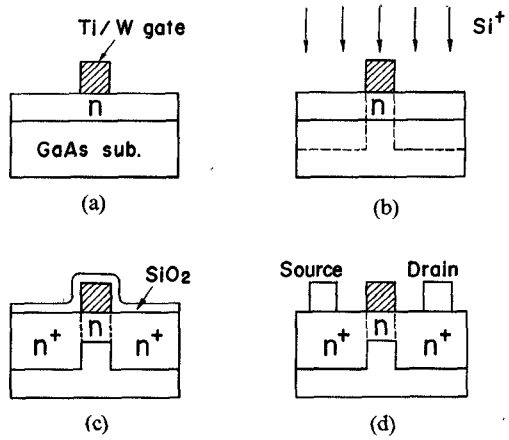

Fig. 1. Fabrication process of the self-aligned GaAs MESFET. (a) Gate metallization. (b) n^+ implant. (c) SiO_2 deposition and annealing. (d) Ohmic metallization.

The n layers for the GaAs MESFET channels are made by selective Si^+ implantation into a Cr-doped semi-insulating GaAs substrate with a SiO_2 implantation mask at 59 keV with dosages of $1.08\times10^{12}/cm^2$ for the E-MESFET's and $2.16\times10^{12}/cm^2$ for the D-MESFET's, and then by annealing at 850°C for 15 min. The TiW mixture (10:90 wt. %) is deposited by dc sputtering to a thickness of 5000 Å and etching is performed with CF_4+O_2 gas plasma. The Si^+ implant for the n^+ regions is made at 175 keV with a dosage of $1.7\times10^{13}/cm^2$. In this structure, the Schottky-gate reverse breakdown voltage depends mainly on the donor density profile of the n^+ regions, since the n^+ regions are in direct contact with the gate electrode at their boundaries. The ion-implantation energy and the Si^+ dosage are chosen so as to maintain a reverse breakdown voltage of at least 6 V and a peak carrier density of $1\times10^{18}/cm^3$. To realize more stable Schottky-diode characteristics, TiW silicide gate technology has been developed for and successfully applied to gate metallization of self-aligned fully implanted E/D-mode GaAs MESFET in 1024-bit GaAs fixed address static memory cell array [9].

For the self-aligned E-MESFET with a gate length of 1.5 μm, a gate width of 1 mm, and a threshold voltage of +0.05 V, a source series resistance r_s of 0.75 Ω is obtained, with a transconductance g_m of 87 mS/mm at a gate voltage of +0.6 V. Compared with the performances of r_s of 3.8 Ω and g_m of 30 mS/mm in the conventional E-MESFET, r_s is 20 percent smaller and g_m is about three times larger. The self-aligned MESFET is also superior in packing density, because it has a completely planar structure which does not require accurate gate alignment.

Fig. 2 compares the speed–power performance of self-aligned GaAs E-MESFET logic with that of current GaAs MESFET logics, including 1978 data for GaAs D-MESFET logics [3]. The heaviest line shows the performance of the 1.5-μm gate self-aligned E-MESFET logic. The minimum switching time is 50 ps, and the lowest power-delay product is 14.5 fJ. This switching time is the same as that of recent data for 1.0-μm gate D-MESFET logic ($\tau_d\approx52$ ps at

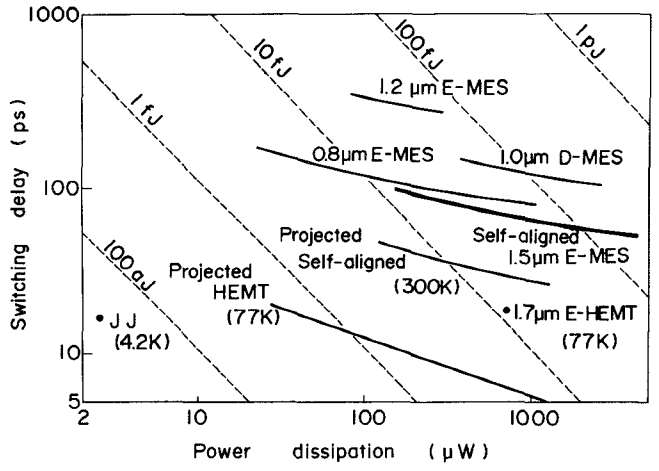

Fig. 2. Speed and power performance of the self-aligned GaAs MESFET logic compared with current GaAs MESFET logic, HEMT logic, and Josephson Junction logic.

a 1 mW/gate power dissipation), and the power-delay product is several times smaller for a switching time of 100 ps, and these values compare favorably to those of 0.8-μm gate E-MESFET logic [10]. Projected performance of self-aligned 1-μm gate E-MESFET logic is also shown in this figure. A switching time of 40 ps with a power dissipation of 1 mW will be achieved at room temperature operation. As described above, the self-aligned GaAs MESFET technology is a very promising means of achieving high-speed logic and static RAM if the E-MESFET characteristics can be controlled precisely.

III. HEMT Technology

HEMT technology has new possibilities towards LSI/VLSI with high speed and low-power dissipation. We have already developed E/D-mode HEMT's [11], [12], and successfully integrated E/D-type DCL circuits [13]. Fig. 3 shows the cross sectional view of the D-HEMT, with a selectively doped GaAs/AlGaAs heterojunction structure. A nondoped GaAs layer and Si-doped n-type AlGaAs layer are successively grown on a semi-insulating GaAs substrate by MBE. Because of the higher electron affinity of GaAs, free electrons in the AlGaAs layer are transferred to the nondoped GaAs layer, where they form a two-dimensional high-mobility electron gas within 100 Å of the interface.

Fig. 4 shows the energy-band diagram of the D- and E-HEMT's in the thermal equilibrium (without bias). The n-type AlGaAs layer of the D-HEMT is completely depleted in two depletion mechanisms: 1) the surface depletion results from the trapping of free electrons by surface states; and 2) the interface depletion results from the transfer of electrons into the nondoped GaAs. The Fermi level of the gate metal is matched to the pinning point, which is 1.2-eV below the conduction band. With the reduced AlGaAs layer thickness, the electrons supplied by donors in the AlGaAs layer is insufficient to pin the surface Fermi level. Therefore, the space charge region extends into the nondoped GaAs layer and, as a result, band bending results in the upward direction, and the

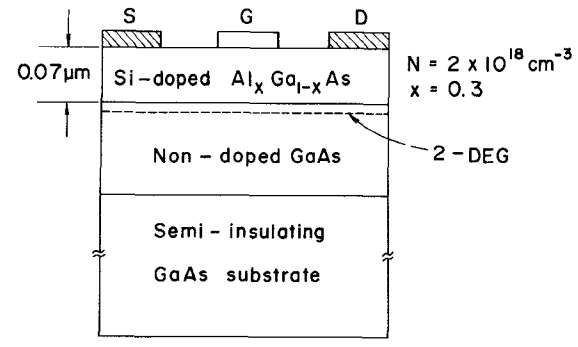

Fig. 3. Cross-sectional view of the depletion mode HEMT.

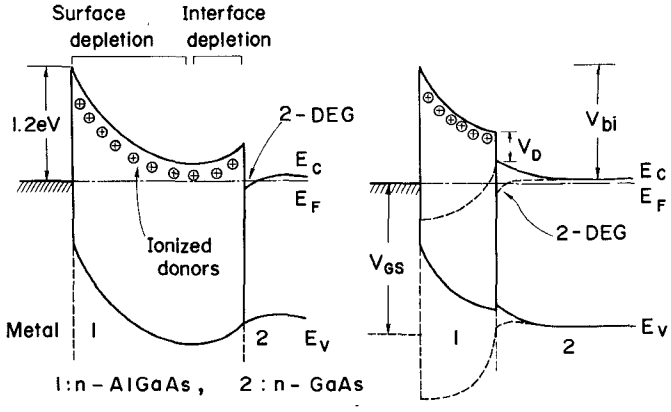

Fig. 4. Energy-band diagram of the (a) D- and (b) E-HEMT's.

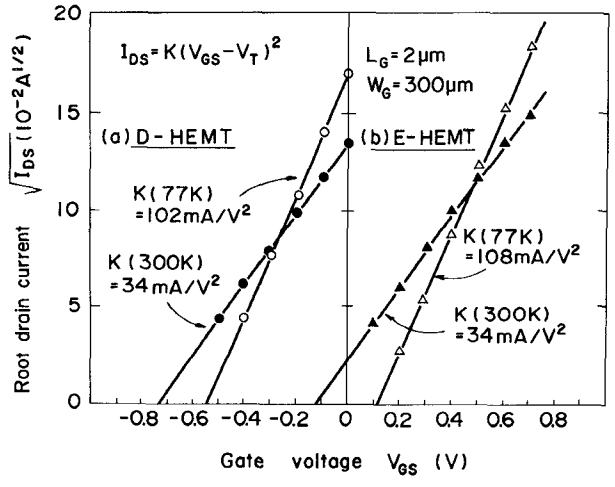

Fig. 5. Transfer characteristics of the square root of the drain saturation current versus gate voltage of the D- and E-HEMT's.

two-dimensional electron gas disappears, as understood in this figure. When a positive voltage V_{GS} higher than the threshold voltage is applied to the gate, electrons accumulate at the interface and form a two-dimensional electron gas, as shown by the broken lines. Thus, we can have the E-HEMT.

In Fig. 5, transfer characteristics of the square root of the drain saturation current versus gate voltage, $\sqrt{I_{DS}}$ versus V_{GS}, are plotted for both the E- and D-HEMT's. Both devices exhibit the square law $I_{DS} = K(V_{GS} - V_T)^2$

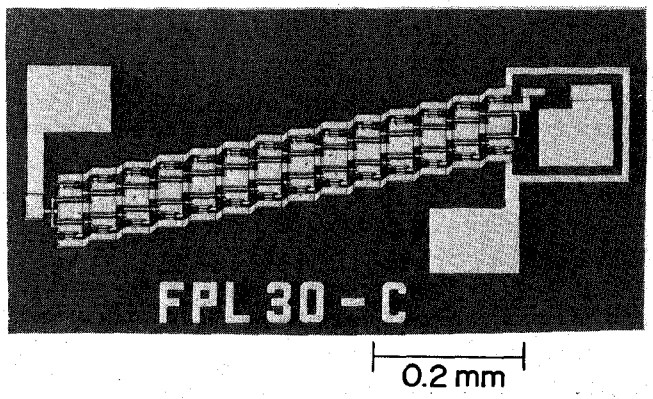

Fig. 6. Fabricated 27-stage HEMT ring oscillator with an output buffer and a probe resistor.

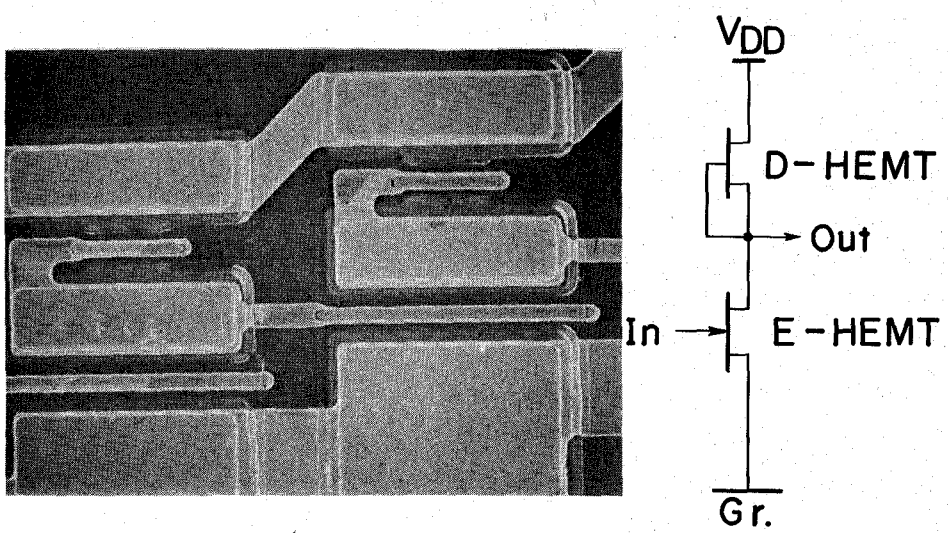

Fig. 7. Magnified microphotograph of a HEMT inverter.

characteristics. The K-value is given by $\epsilon\mu_n W_G/2aL_G$ in the low-field region. Here, ϵ is the dielectric constant of the $Al_XGa_{1-X}As$ layer, μ_n is the field-effect mobility, and a is the thickness of the $Al_XGa_{1-X}As$ layer ($a \simeq 0.07$ μm in Fig. 5). By lowering the temperature to 77 K, a dramatic increase in K-value by a factor of 3 is observed. This increase in K-value is due to the increase in electron mobility at low temperatures. The low-field electron mobility was found from Hall measurements to be around 6000 $cm^2/V\cdot s$ at 300 K and around 20 000 $cm^2/V\cdot s$ at 77 K, though the experimental K-values of Fig. 5, with the formula above, yields effective channel mobilities in the HEMTs of about half of these values. It is important to note here that the degree of improvement (3 times) in K-value at 77 K is about the same as that of the low-field electron mobility at 77 K, although the K-value is measured in the high-field region (the average field within the channel: ~ 4 kV/cm) where the velocity saturation effects become very significant. Low-field mobilities of 117 000 $cm^2/V\cdot s$ at 77 K, and 244 000 $cm^2/V\cdot s$ at 5 K with a sheet electron concentration of about $4.9\times10^{11}/cm^2$ have already been achieved [14]. More recently, a mobility of one million $cm^2/V\cdot s$ has been achieved at 5 K under photo excitation. At $V_{DS}=1.5$ V and $V_{GS}=0.7$ V, the E-HEMT exhibits g_m of 193 mS/mm at 300 K and g_m increases to 409 mS/mm at 77 K. This value of g_m at 77 K is the highest ever reported for any field-effect devices.

Fig. 6 shows a microphotograph of a 27-stage ring oscillator fabricated with E-mode switching and D-mode load HEMT's, with a fan-in and fan-out of one. The gate length of the switching HEMT is 1.7 μm. Fig. 7 shows a magnified microphotograph of the HEMT inverter. Relatively wide switching devices (33 μm) are used to minimize the effect of wiring capacitance. The gate width of the D-mode load devices was adjusted to 7 μm for room temperature operation. Since the K-value of the switching device increases by more than a factor of 2 at liquid nitrogen temperature, the gate width of the load devices was increased to 13 μm for devices designed for low temperature operation to give the desired higher current.

The power dissipation of a room temperature device with a gate length of 1.7 μm is 0.46 mW, significantly less than that of currently achievable GaAs MESFET logics with a comparable gate length at the same switching time (56.5 ps). This superiority in speed–power performance of the room temperature device over GaAs MESFET logic

results partly from the higher electron mobility (6000 $cm^2/V \cdot s$) of the HEMT as compared to the MESFET (4500 $cm^2/V \cdot s$). At liquid nitrogen temperature, the switching time of 17.1 ps, with the power dissipation of 0.96 mW, has been achieved. The power dissipation of 0.96 mW at liquid nitrogen temperature is two times higher than at 300 K due to the increased current from the wider gate of the D-mode load devices designed for 77 K operation. The switching time of 17.1 ps is the lowest in Si and GaAs logic technologies ever reported and is comparable with that of Josephson Junction logic (13 ps) [15]. More recently, switching times of 16.7 ps per stage at room temperature and 12.8 ps per stage at liquid nitrogen temperature have been achieved in the 27-stage ring oscillator with E-HEMT of 1.1-μm gate length. The speed–power performances of HEMT logic are included in Fig. 2. Taking into account the results of 1.7-μm gate HEMT technology, 1-μm gate HEMT logic with an improved mobility of about 60 000 $cm^2/V \cdot s$ can be expected to achieve a switching delay of 10 ps with about 100-μW power dissipation per stage at liquid nitrogen temperature.

IV. Projected System Performances

System performances for the mainframe of a future computer are projected and discussed, based on the results on self-aligned MESFET and HEMT logics described in Sections II and III.

Today's computer systems are constructed by stacking printed circuit boards. Fig. 8 shows chip layout on the board, logic layout on the chip, wiring on the chip, and external wiring between chips. System delay mainly results from two sources: chip delay and external wiring delay. The chip delay time τ can be estimated from the simplified model, i.e., $\tau = k(C_l + mC_{in})/p_t$, where k is constant, C_l is the line capacitance, C_{in} is the gate–source capacitance, and m is the number of fan-out.

Using the experimental data and the conditions of $C_l = 0$ and $m = 1$, for self-aligned MESFET and HEMT of Fig. 2, the k values are determined as 0.14 for HEMT and 0.56 for self-aligned MESFET, respectively. As a result, the chip delay can be calculated by assuming $C_l = 60$ fF and $m = 2.5$, as a function of power p_t, as shown in Fig. 9. The power p_t of internal gate is limited by the total chip power P_t and the number of gates per chip, i.e., $P_t = n_e p_e + n_t p_t \equiv Qa^2$. Here, p_e is the power of external gate to excite the external load including stray capacitance of transmission line (p_e is assumed to be 10 mW), n_e is the number of terminals required to connect external wiring, n_t is the number of internal gates, Q is the heat flux and assumed 20 W/cm^2 for liquid cooling, and a is the chip size. For a 10-kilogate integration, p_t of 1.2 mW is obtained under a of 8 mm and n_e of 100. As a result, chip delays per gate of 100 ps and 30 ps can be derived from the curves of Fig. 9 for the GaAs MESFET and HEMT, respectively.

Fig. 10 shows the chip delay per gate as a function of the number of gates per chip. External wiring delay is determined by the length of the external wiring network, depending on the pitch between chips and packing technology, and is assumed in the broken line shown in Fig. 10. Fig. 11 shows the system delay per gate which is the sum of the chip delay and the external wiring delay shown in Fig. 10. For small-scale integration, the most delay results from the external wiring. For large-scale integration, on the other hand, the chip delay is predominant. Optimum system performances are system delays of 200 ps at 10

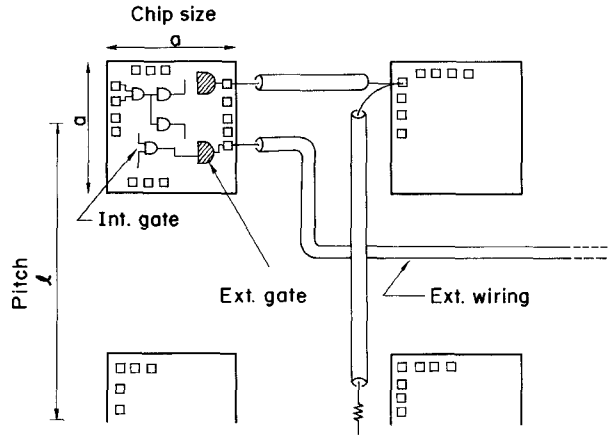

Fig. 8. Schematic illustration of the chip layout on the board in the computer system.

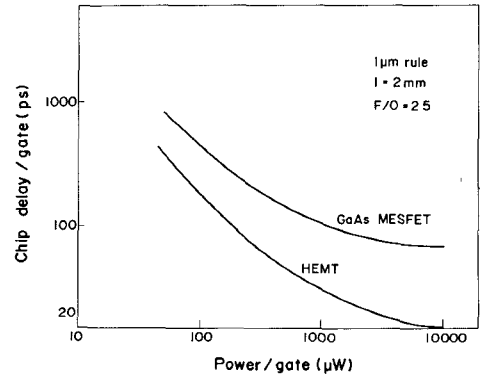

Fig. 9. Chip delay calculated as a function of the power of internal gate.

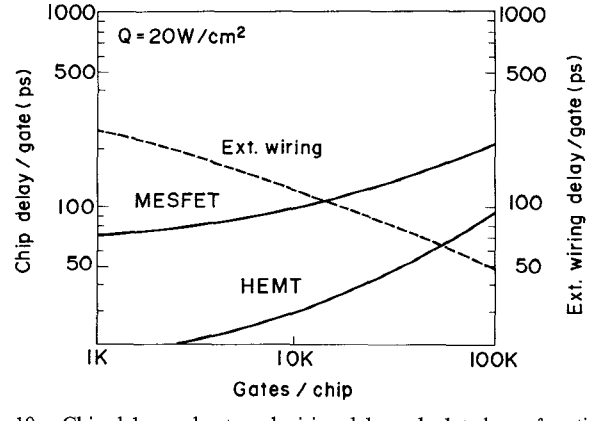

Fig. 10. Chip delay and external wiring delay calculated as a function of the number of gates.

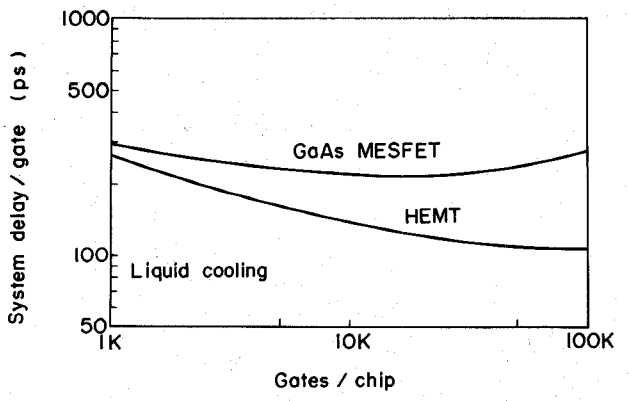

Fig. 11. Projected system delay calculated as a function of the number of gates.

kilogates for GaAs MESFET VLSI, and 100 ps at 100 kilogates for HEMT VLSI.

V. Conclusion

For future large-scale computer applications, the performance of 100 MIPS with a system delay per gate of below 200 ps is required. To satisfy this high-speed requirement, new device technologies aimed at GaAs VLSI have been developed. The self-aligned fully implanted planar GaAs MESFET logic with 1.5-μm gate length exhibits a switching time of 50 ps at room temperature. The E/D type direct coupled HEMT logic with 1.7-μm gate length has achieved a switching time of 17.1 ps at liquid nitrogen temperature, the highest speed of any semiconductor device logic ever reported. Projected switching performance of HEMT logic with 1-μm design rule technology shows it to be superior to that of Josephson Junction logic. More recently, 1.1-μm gate HEMT logic has achieved a switching time of 12.8 ps, which demonstrates higher speed than the top speed of Josephson Junction logic. With the experimental data on the self-aligned MESFET and the HEMT logics, optimized system performances are projected to system delays of 200 ps at 10-kilogate integration with GaAs MESFET VLSI, and 100 ps at 100-kilogate integration with HEMT VLSI.

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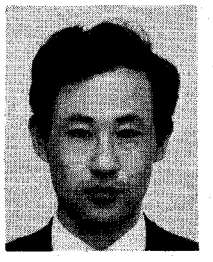


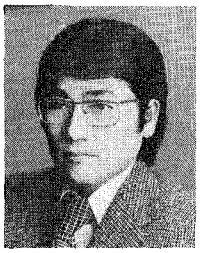
Masayuki Abe (M'74) was born in Fukushima, Japan, on January 7, 1941. He received the B.E., M.E., and Ph.D. degrees in electrical engineering from Osaka University, Osaka, Japan, in 1967, 1969, and 1973, respectively.

His research has included high electric-field transport in semiconductors, especially dynamic characteristics of hot electrons in GaAs. In 1973 he joined the Fujitsu Laboratories Ltd., Kawasaki, Japan, where he was engaged in Gunn-effect logic devices and Monte Carlo simulation of Gunn-domain dynamics. From 1975 to 1980 he was engaged in developing thick-window high-radiance GaAlAs and InGaAsP LED's for fiber-optical communications. In 1980 he received the Paper Award of the Laser Society of Japan for "GaAlAs Monolithic Lensed LED." Since 1980 he has been engaged in developing GaAs IC's and HEMT. He is currently Section Manager of Semiconductor Devices Laboratory, Fujitsu Laboratories Ltd.

Dr. Abe is a member of the Institute of Electronics and Communication Engineers of Japan and the Japan Society of Applied Physics.

Takashi Mimura (M'73) was born on December 14, 1944. He received the B.S. degree in physics in 1967 from the Kwanseigakuin University, Nishinomiya, Japan, and the M.S. degree in solid-state physics, in 1970, from Osaka University, Osaka, Japan.

In 1970 he joined the Fujitsu Ltd., Kobe, Japan, where he had



worked on research and development of silicon and gallium arsenide microwave devices, including planar analog transistors. In 1975 he transferred to the Fujitsu Laboratories, Ltd., Kawasaki, Japan, where he has been engaged in the research and development of compound semiconductor high-speed devices, including high electron mobility transistors (HEMT's). In 1981 he received the prize of the Minister of Science and Techniques in Japan for the invention of a HEMT.

Mr. Mimura is a member of the Physical Society of Japan.

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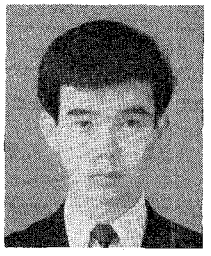

Naoki Yokoyama (M'78) was born in Osaka, Japan, on March 28, 1949. He received the B.S. degree in physics from Osaka City University, Osaka, Japan, and the M.S. degree in physics from Osaka University, Osaka, in 1971 and 1973, respectively.

In 1973 he joined the Semiconductor Laboratory, Fujitsu Laboratories, Ltd., Kawasaki, Japan, where he has been engaged in the research and development of GaAs field-effect transistors and GaAs digital integrated circuits.

Mr. Yokoyama is a member of the Physical Society of Japan, the Japan Society of Applied Physics, and the Institute of Electronics and Communication Engineers of Japan.

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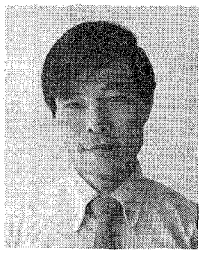

Hajime Ishikawa (M'77) was born in Kurashiki, Japan, on February 11, 1939. He received the B.E. degree in electrical engineering from Tohoku University, Sendai, Japan, in 1961.

He joined Kobe Industries Co., which later merged with Fujitsu Laboratories Ltd., Kawasaki, Japan. Since then he has been working on the research of surface physics of semiconductors, developing microwave communication systems and developing semiconductor devices including Si low-noise and high-power bipolar transistors and GaAs low-noise and power MESFET's. He is presently engaged in the development of MOS integrated circuits.

Mr. Ishikawa is a member of the Institute of Electronics and Communication Engineers of Japan and the Electrochemical Society.

A GaAs MSI Word Generator Operating at 5 Gbits/s Data Rate

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Abstract—**This paper describes a monolithic MSI GaAs word generator that operates at data rates from a few bits/s up to 5 Gbits/s. This circuit, with 600 active devices, consists of an 8:1 parallel-to-serial converter, a timing generator, control logic, and ECL-interface networks. The circuit generates multiple 8-bit words with dynamic word-length control. The paper discusses the fabrication technology, the design of the word generator and its building blocks, and the performance of the complete chip.**

I. INTRODUCTION

FUTURE high-speed digital electronic systems, such as fiber-optic communication networks or radar signal processors, will require test instruments that generate, receive, and analyze data at rates greater than 1 Gbits/s. These needs can be met with GaAs monolithic-integrated circuits that operate at clock frequencies beyond the reach of present silicon IC's. The principal requirements for these GaAs circuits in test instrumentation are as follows:

1) short gate delays and fast rise and fall times (<100 ps) for full logic swings;

2) minimum switching time jitter (e.g., minimum phase noise in digital frequency dividers [1]);

3) compatibility with ECL families;

4) stable and reliable operation with adequate noise margins;

5) sufficient level of complexity to allow useful test circuits to be realized (100 to 1000 devices per chip);

6) reasonable power dissipation per chip (<2 W); and

7) high fabrication yield in order to be cost-effective.

Among the most useful circuits for test instrumentation having the above applications and requirements are pro-

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